IN THE CLAIMS:

1. A system on chip (SOC) DC voltage generator system for supplying at least one voltage level to a plurality of subsystems on a chip having an SOC design, each of the subsystems having a plurality of units, the DC voltage generator system comprising:

a plurality of local DC voltage generators distributed throughout the chip, each local DC voltage generator independently supplying voltage to at least one unit of the plurality of subsystems, each local DC voltage generator including:

at least one regulator system incorporated in a section of the local DC voltage generator, a power control unit and a clock control unit, wherein each regulator system receiving a clock control signal from said power control and clock control units and outputting one pump control signal from the section of the local DC voltage generator, the pump control signal being based on the clock control signal; and

a pump system receiving the one pump control signal and outputting at least one voltage level in accordance with the one pump control signal.

2. The SOC DC voltage generator system according to Claim 1, wherein each local DC voltage generator is located proximate to a unit of the plurality of units.

3. The SOC DC voltage generator system according to Claim 1, wherein each local DC voltage generator supplies the voltage level to one unit of the plurality of units.

4. The SOC DC voltage generator system according to Claim 1, wherein a voltage level of the voltage supplied is selectable.

5. The SOC DC voltage generator system according to Claim 1, wherein each local DC voltage generator is independently controlled by a respective control signal.

6. The SOC DC voltage generator system according to Claim 5, wherein each respective control signal is generated by a power control unit in accordance with a power level mode at which the chip is operating.

7. The SOC DC voltage generator system according to Claim 6, wherein the power control unit receives instructions from an external source for determining the power level mode.

8. The SOC DC voltage generator system according to Claim 5, wherein each respective control signal is generated by a clock control unit.

9. The SOC DC voltage generator system according to Claim 5, wherein each respective control signal is generated in accordance with an activity level of the chip.

10. The SOC DC voltage generator system according to Claim 9, wherein the activity level is one of a switching activity level and an I/O activity level.

11. The SOC DC voltage generator system according to Claim 8, wherein the respective control signal controlling one of the local DC voltage generators is provided to the unit associated with the local DC voltage generator.

12. The voltage generator system according to Claim 5, wherein each respective control signal controls current flow in the local DC voltage generator.

13. A method for supplying voltage to a plurality of subsystems on a chip having an SOC design, each of the subsystems having a plurality of units, the method comprising the steps of:

distributing a plurality of local DC voltage generators throughout the chip;

supplying a clock control signal to each of the local DC voltage generators;

generating, in a section of each local DC voltage generator, a pump control signal;

receiving, with a pump system of each local DC voltage generator, the pump control signal;

generating, using the pump system, a DC voltage based on the pump control signal; and

supplying the generated DC voltage to the plurality of units of said plurality of subsystems.

14. The method of Claim 13, further comprising the step of independently controlling each local DC voltage generator of the plurality of DC voltage generators.

15. The method of Claim 13, further comprising the step of independently selecting a voltage level to be supplied by each local DC voltage generator.

16. The method of Claim 14, wherein the step of independently controlling includes controlling each local DC voltage generator in accordance with a power mode of the chip.

17. The method of Claim 17, wherein the step of independently controlling includes controlling each local DC voltage generator in accordance with a clock control signal.

18. The method of Claim 17, wherein the clock control signal is further provided to selected units of the plurality of units.

19. The method of Claim 14, wherein the step of independently controlling includes controlling each local DC voltage generator in accordance with an activity level of the chip.

20. The method of Claim 19, wherein activity level is one of a switching level and an I/O level of the chip.

21. The method of Claim 1, wherein the pump control signal is based on the clock control signal to accommodate different system operating modes selected from one of high performance mode and low-power mode.